REMARKS

This Amendment is in response to the Office Action mailed July 16, 2003.

Claims 10-13 are presented for examination are rejected under 35 USC 102(b) as being anticipated by Shobatake et al. (U.S. Patent No. 5,557,609). To support the rejection the Examiner argues that the reference, among other things, teaches storing in an instruction memory instructions for the handling of data transiting an interface device and executing in a plurality of interface processors the instructions stored in the instruction memory. The Examiner points to Figure 1, column 3, line 56 to column 4, line 56 for teaching storing in an instruction memory instructions for handling of data transiting an interface device and executing in a plurality of interface processors the instructions stored in the instruction memory.

In response, applicants traverse the rejection and argue, among other things, storing in an instruction memory instructions for the handling of data transiting an interface device and executing in a plurality of interface processors the instructions stored in the instruction memory are not disclosed or suggested in the portion of the reference specifically identified by the Examiner or in any other part of the reference. Contrary to the Examiner's position the reference teaches a plurality of interface processors 102-1 through 102-N coupling individual ports of a switching system to the switch. As set forth at column 4, lines 40-56, each of the Interface processors has a main memory only one of which is shown and number 11023 in Fig. 1. As stated in column 4, lines 52-55, "The processor 11021 includes an ALU and a sequencer used for channel-processing in the present invention, and further a channel

processing procedure code executed by the processor 11021 is written in the main memory 11023." Because the reference clearly teaches that each of the interface processors 1002-2 through 102-N are structured as the one shown in 102-1 it is clear that each of these processors has its own main memory from which it executes instructions as set forth at column 4, lines 52-55. Therefore, contrary to the Examiner's position and insofar as the claim is modified for clarity the reference does not show executing in a plurality of interface processors the instructions stored in the instruction memory.

It is settled law[1] that in order for a reference to anticipate claims under 35 USC 102(b) every process step recited in the claim must be shown in the reference. As argued above, "executing in a plurality of interface processors the instructions stored in the single instruction memory is not disclosed in the reference". Therefore, the reference does not anticipate the claim. Likewise, "storing in a single instruction memory instructions for the handling of data transiting an interface device is not shown in the reference".

Newly added claims 43 and 44 are patentable over the art of record for the reasons set forth above.

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[1]Citation omitted but can be provided if necessary.

PATENT
IBM Docket No. RAL999-0080

It is believed that the present amendment answers all the issues raised by the Examiner. Reconsideration is hereby requested and an early allowance of all the claims is solicited.

Respectfully Submitted,

Joscelyn G. Cockburn

Joscelyn G. Cockburn
Reg. No. 27,069
Attorney of Record
IBM Corporation
IP Law Dept. 9CCA/B002
P.O. Box 12195
Research Triangle Park, NC 27709

JGC:ko
919-543-9036
FAX 919-254-2649